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Digital "Noise" Common-mode Coupling Mechanisms in the Z-Axis (*)

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Introduction

The development of "digital common-mode noise" within circuit devices and subsequently within circuit boards, is initially formed by peak over-shoot and under-shoot currents in the power and return planes. The peak currents are attributable to the "cross-conduction" transitions in circuit devices, where literally the driver segments turning "on" do so before the pull-down drivers turn "off".

The result is that at each and every rise and fall time, a partial "short circuit" is found across the output rails across the driver sets. When compared to the total signal output current driven by a circuit device, the "peak power current" may be 5 to 10 times higher in amplitude. These effects are displayed by **Figure One**.

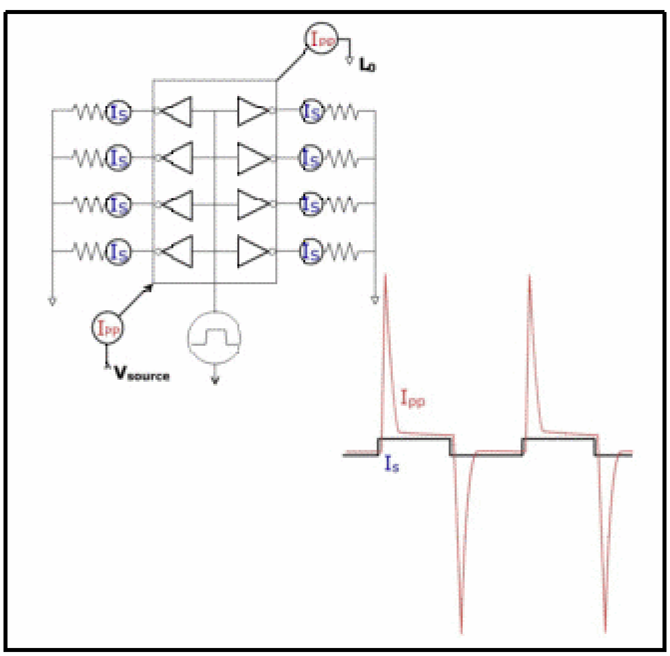

Figure One
Comparative Overlay of Accumulated Signal Currents (**I_s**) to
Peak Power Common-mode Currents (**I_{pp}**).
Currents (**I_{pp}**) May Be Exhibited As Several Amperes Compared To
Amplitudes Of Accumulated Milliamperes For Signal Currents (**I_s**).

Common-mode Regions: Devices and Circuit Boards

As a result of the accumulated common-mode currents, common-mode fields are produced in essentially two regions: a) the pattern of inductance presented by signal-escapes into the ground and power planes that circumscribe circuit devices; and b) the packaging of each circuit device, as suggested by **Figure Two**.

The process of developing "distributed inductance" in the circuit board circumscription of circuit devices, is called "patterned layout inductance". The inductance is derived from the array of "holes" (sometimes termed "anti-pads") in the clearance required in the planes for signals in vias to pass through. Generally, the denser the hole pattern in the planes, the more inductance will be equivalently formed.

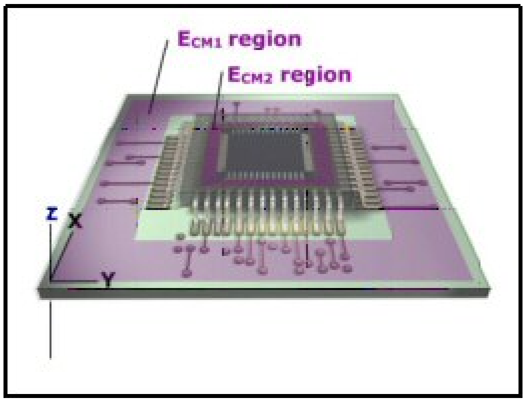

Figure Two

Illustration Of Primary Common-mode Field Potential Regions:
E_{CM1} Around Patterned Layout Inductance; E_{CM2} Within Losses In Circuit Device Packaging

Z-Axis Coupling Within Circuit Boards

The effect of common-mode coupling into signal partitions through the stack-up of circuit boards as a result of the cross-conduction “peak power currents”, is dependent upon the sequence of the stack-up itself. As suggested by **Figure Three**, when power (Voltage) and image (return) planes are placed far apart when and separated by signal layers, a process of flux induction may occur into the “drilled signal vias” as signal paths themselves. The coupling process would be such that ,in impact causing power flux induction into signals would be caused, taking in a dynamic form of series modulation. The effect is noted because when a power plane is separated from its image plane, the common-mode current eddy across the apertures (holes) in the planes will set up a flux-pattern similar to that as an array of small loop antenna structures. While the phase relationship of the “holes as loop antennas” between the power and image planes would attempt to mutually cancel inductance, the distance separation causes this to be less efficient than when the two planes would be co-located as directly adjacent as indicated by **Figure Four**, which would dynamically improve the result. When the stack-up results in inefficient cancellation, Z-Axis fields (**E_{CM}**) may be developed, resulting in coupling within the circuit board in the same axis. Efficient choices for stack-ups can mitigate the effects and improve performance for signal quality, S/N ratios and EMC performance.

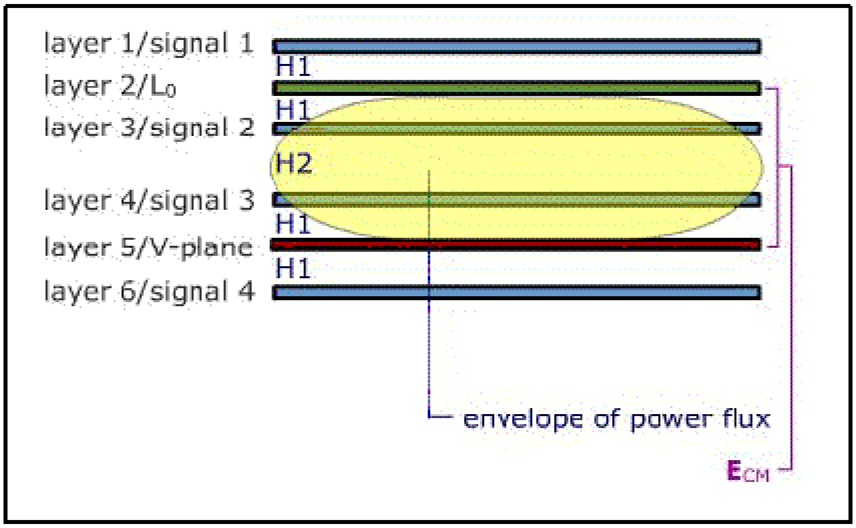

Figure Three-A
Inefficient Stack-Up Of Planes for Flux Cancellation

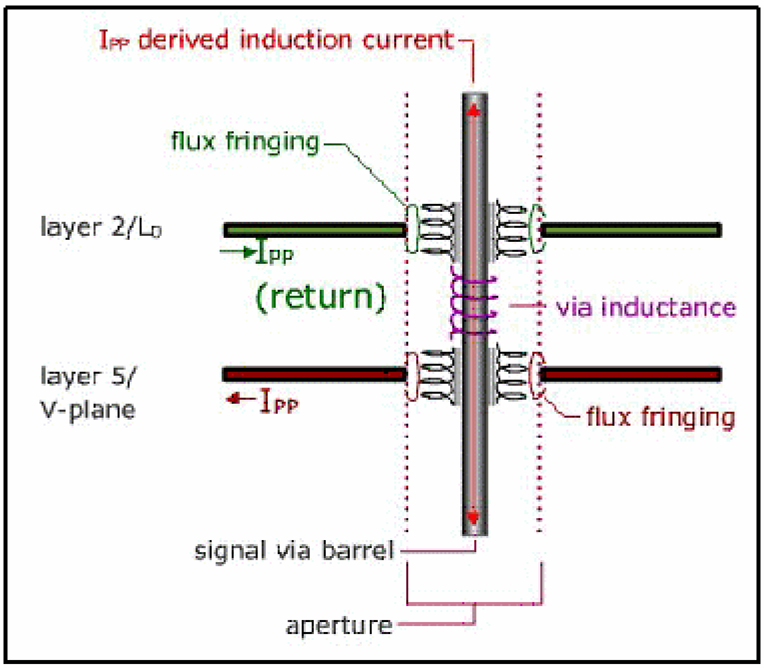

Figure Three-B
Flux Induction Into Vias Implies Series Superimpositions Of “Noise” Modulation

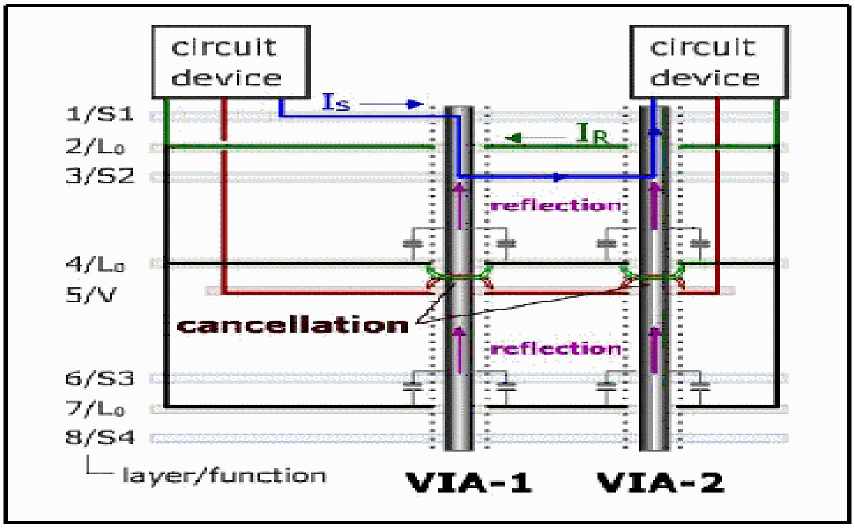

Figure Four
Efficient Flux Cancellation Can Null Common-mode Induction Fields

Z-Axis Coupling With Respect To Packaging And Other Circuit Boards
When fields with related potentials are developed across the X-Y axis of circuit boards, the fields will couple to conductive chassis members or to other circuit boards which are located in close proximity. The coupling transfer functions may be described: a) as the equivalence equivalent of a “distributed transmission line” in the structure of asa lattice; or, b) as a near-field effect, magnetic- field dominant, electromagnetic wave transfer.

Figure Five initiates the description of these processes by illustrating the circuit-equivalent of the formation of the circuit board contribution to the distributed line parameters.

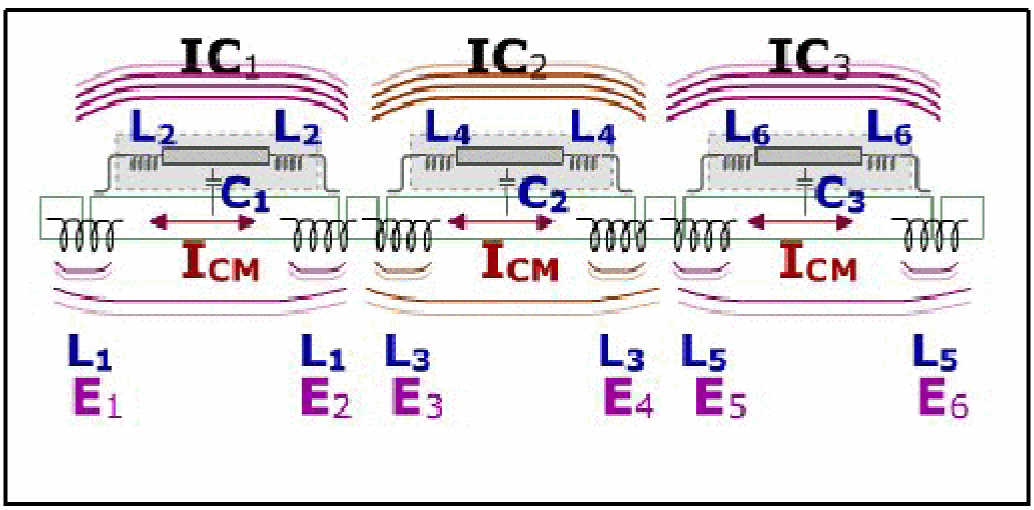

Figure Five
Initial Formation of Distributed Transmission Line Structure Components
Derived From "Pattern Layout Inductance" of Circuit Board

As depicted in **Figure Five**, the patterned layout inductance circumscribing each "IC" circuit device become excited through the common-mode peak power currents, $\mathbf{I_{CM}}$. This results in a sequence of field potentials, $\mathbf{E_1}$ through $\mathbf{E_6}$ across the cross-section of the circuit board. Apart from the electrical field potentials that occur as a function of E = L di/dt (that cause $\mathbf{E_1}$ through $\mathbf{E_6}$), Electromagnetic Fields are developed. These fields propagate respectively from: a) the IC "packages" above the circuit board; b) locally from the "small loop antenna arrays" presented as the "via holes"; and, c) across the larger displacements of the "patterns" of the "hole arrays" around the perimeters of the circuit devices.

It might be intuitively obvious that the structure of the "distributed line" is not adequately defined by a simple cross-section through a circuit board. In actuality, the "distributed line" can be considered in three axes, in the form of a lattice. The concept of the lattice is displayed by **Figure Six**.

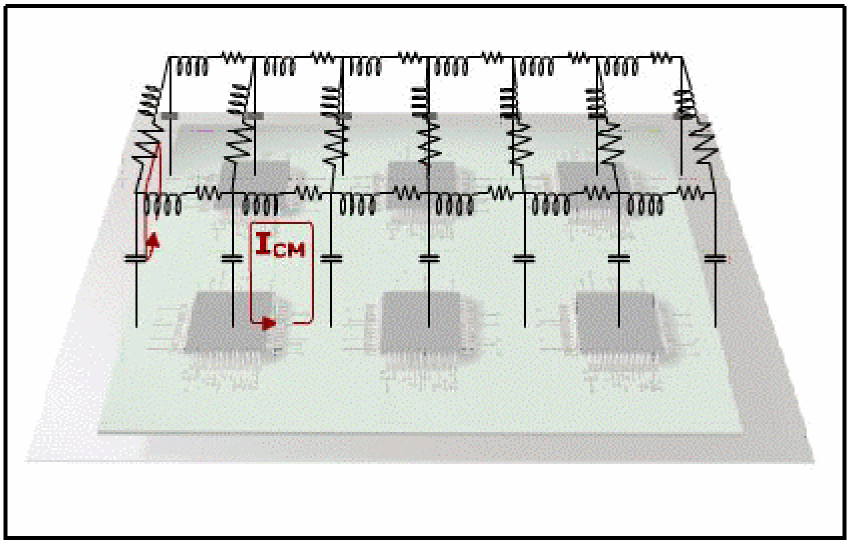

Figure Six
Conceptual View of Distributed Transmission Line Components
Structured As A Lattice In Three Axes

For clarity, the concept of the "lattice structure" is illustrated as being located above the circuit board. It is important to note, however, that the distributed capacitance will be presented in the distance separation underneath the circuit board to the chassis plane, not above it. (It is also true, however, that if a conductive structure were to be placed above the circuit board, distributed capacitance would also be established across that dimensional separation.)

The concepts of the descriptions as a "distributed transmission line" that is initially may be observed in the examples of **Figures Five** and **Six** noted both in terms of current and common-mode fields transfers as a sequence cution across the two boundaries of "the distributed line" (circuit board and chassis plane) . When the distributed common-mode field potentials are formed, ($\mathbf{E_1}$ through $\mathbf{E_6}$ across the cross-section of the circuit board) essentially any other conducted structure connected or coupled to the circuit board will experience common-mode derivative currents ($\mathbf{I_1}$ through $\mathbf{I_6}$) and potentials ($\mathbf{E_{CM1}}$ through $\mathbf{E_{CM6}}$) which are conveyed from the source board initially by distributed capacitance. This interaction can influence the signal-noise ratios among elements of the product by the propagation of these common-mode eddy currents across the distributed line. If considered as an electromagnetic wave transfer, it is noted that circuit boards (comprised of low power impedances with high spectral currents) would displace magnetic-field dominant near- field effects. **Figure Six** suggests the equivalent wave impedance profiles that would be exhibited in the coupling mechanisms in this mode of transfer.

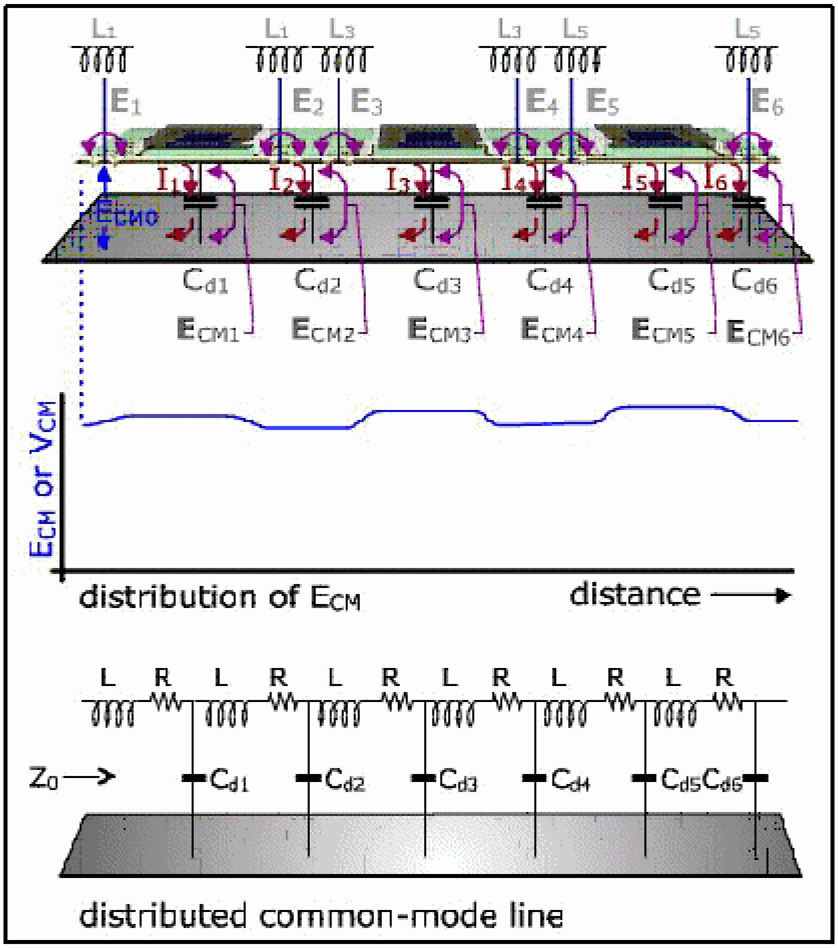

Figure Seven
Display of Distributed Transmission Line
With Field Potential "Map" And Common-mode Current Displacements

To gain a further concept of the potential coupling and interactions that are related to these common-mode transfers, the illustration of **Figure Eight** is provided. It may be recognized that the simple addition of two unshielded conductors (or cables) to opposing edges of the circuit board cross section, will immediately result in the development of several (approximately 5) antenna structures. These are: Monopole "A"; Monopole "B"; Dipole "C"; Circuit Devices (represented as an array) "D"; and the Slot Structure established between the parallel planes, "E". In these views, a dynamically active circuit board simply placed above a conductive plane with two connected wires or cables, may actually construct a multi-mode interactive (and co-dependent) antenna array. This array would be highly interactive in mutual influences of "noise" (and intrinsic EMC issues within a system-product) with related potentials and currents both across the circuit board as well as into the connected wires and cables.

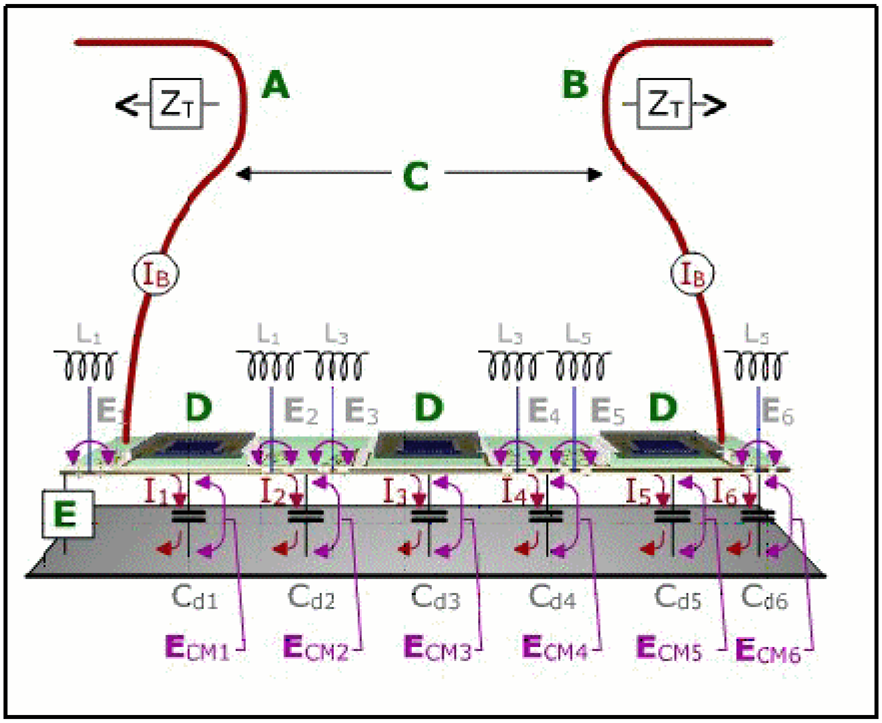

Figure Eight
Interactive Antenna Structures Can Mutually Cross-Couple Common-mode Potentials

In order to further expand this discussion, the process of these transfers will also be related to the impedance and presence of electromagnetic waves that are propagating between the boundaries. For brevity, when an impedance that is initially formed through distributed capacitance becomes excited by electrical potentials, a current is formed across (through) the capacitance as a distributed electromagnetic coupling and transfer mechanism. The impedance of this electromagnetic wave transfer ($\mathbf{Z_W}$) will be related to the magnitude of the electric field intensity divided by the current intensity. This essentially follows Ohm's law, where a spatial term is added to provide a uniform standard of dimension in the form of $\mathbf{Z_W}$ = E-Field Intensity (in Volts/Meter) / H-Field Intensity (in Amperes/Meter). In practice, electromagnetic waves exist through various processes that alter the approximate impedance conditions of the wave. These processes are related to the distance of separation from the source of the wave to the point of observation. When this distance dimension is relatively close to the source, the wave condition is said to be in the "near field". Electromagnetic waves that are observed to be in the near field condition tend to display either: higher impedance conditions when in "electric field" dominance modes; or, lower impedance conditions when in "magnetic field" dominance modes.

In order to establish a higher wave impedance electric field dominant condition, the conducted circuit nature of the source of the electromagnetic wave must possess in itself a higher voltage, higher impedance (hundreds to thousands of Ohms), condition. For a lower impedance wave to be developed in the dimensions of the "near field", the current conducted in the source must be of a low impedance, higher current nature. As applied to this discussion, it is noted that circuit boards are comprised of low power impedances (often in the low tens of Ohms to below five Ohms) with high spectral current amplitudes (Amperes to tens of Amperes of $\mathbf{I_{pp}}$). By definition, circuit boards would by necessity of the electrical characteristics displace magnetic-field dominant, near-field wave impedance, propagation effects. **Figure Nine** suggests the equivalent wave impedance profiles that would be exhibited in the coupling mechanisms in this mode of transfer. These transfers are presented with respect to various packaging distances (separations between circuit boards and chassis as the "observation point" of the wave transfer) which extend to rather large distances (> 50 cm).

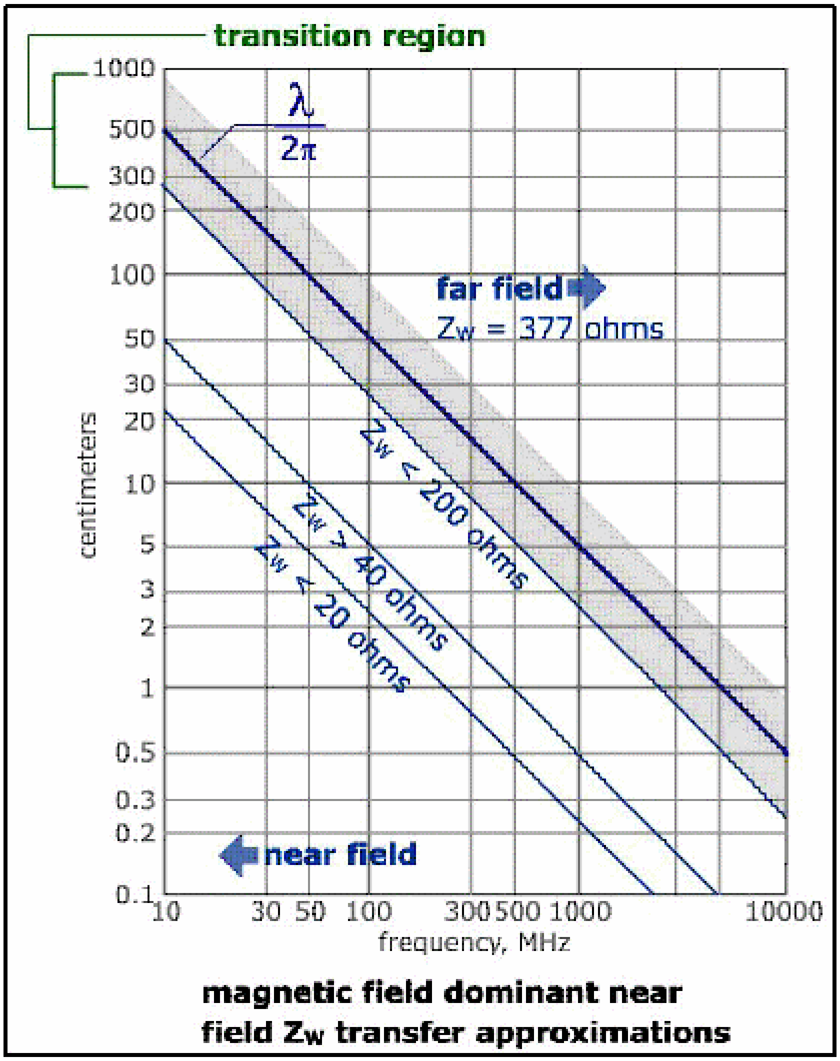

Figure Nine
Approximations Of Magnetic Field Dominant, Near Field, Wave Impedance

Utilizing the representations presented in **Figure Nine**, it is possible to visualize that the processes found across the "distributed transmission line" represented in set up as a lattice, will be (with a very high probability) of a low impedance and intensely interactive nature. In practicality, it would be reasonable to conclude that it is not possible to truly "isolate" a circuit board from a chassis structure at least in terms of broad frequency spectral displacements. To attempt such "isolation" would be to imply defiance of well-established, universally recognized, electromagnetic wave processes! The logical inquiry is simply: "If isolation is not realistically possible, what are the alternatives?".

Control Of Common-Mode Transfers in the Z-Axis
With the recognitions suggested through the coupling concepts described, perhaps the most efficient common-mode Z-Axis control stratagem starts with the recognition that the circuit boards are *not isolated* (i.e. *cannot be* isolated) from conductive chassis!

Apart from efficiently designing the structures, energy storage, and layout of the circuit boards themselves with an emphasis directed to reduced common-mode losses, efficient power delivery to circuit devices and high signal integrity, the transfers from the circuit boards to parallel conductive planes may be controlled using "null" techniques. These "nulls" are devised to set up deliberate "reflections" in the unintended common-mode distributed transmission lines between circuit boards and chassis. Simply said, the idea is to "deflect" through reflections the circulation of common-mode levels toward regions of inefficient coupling whereby signal-to-noise ratios (and EMC performance) may be optimized.

As with all intended "reflection concepts" the magnitude of any intended reflection will be found in the comparative relationship of the impedance values (and position) of the "nulls" compared to the impedance of the "distributed line" itself. Given the suggestions of impedance represented by **Figure Nine** (where wave impedance could approach the low tens of Ohms) the impedance of "nulls" must be significantly lower (e.g., 1 Ohm) in order to be effective. It is noted that in concept, the method of implementing "null reflections" is similar to that of the intended impedance dichotomies found in shielding methods. In shielding theory, the impinging wave impedances are intentionally mismatched by the conductive shield impedance. The first effect of this mismatch causes the electromagnetic waves to be reflected off of the shielding surface and away from the area to be protected from the potentially offending amplitudes conveyed by the wave.

The process of "reflected null implementation" is exhibited in concept by **Figure Ten**. The intention of this technique is to redirect the common-mode transfers to improve signal-to-noise and all effects related to Z-Axis coupling. Note that a "null" is essentially a connection between logic return (L0) and chassis through a low impedance means (e.g., through a short, conductive, circuit board mounting standoff). Nulls "shunt" the potentials developed across the two planes of the distributed transmission line, and reflect the common-mode Z-axis levels away from the null positions. Although in low spectral common-mode distributions (e.g., greater than 500 MHz) nulls may be effective at, or as an array of, specific locations, much higher frequency common-mode spectra may require the use of "null bars" (which are continuous strips) of contiguous regional contact to prevent slot aperture formations at short wavelengths. (Short aperture slot formations may inadvertently become efficient antenna structures.)

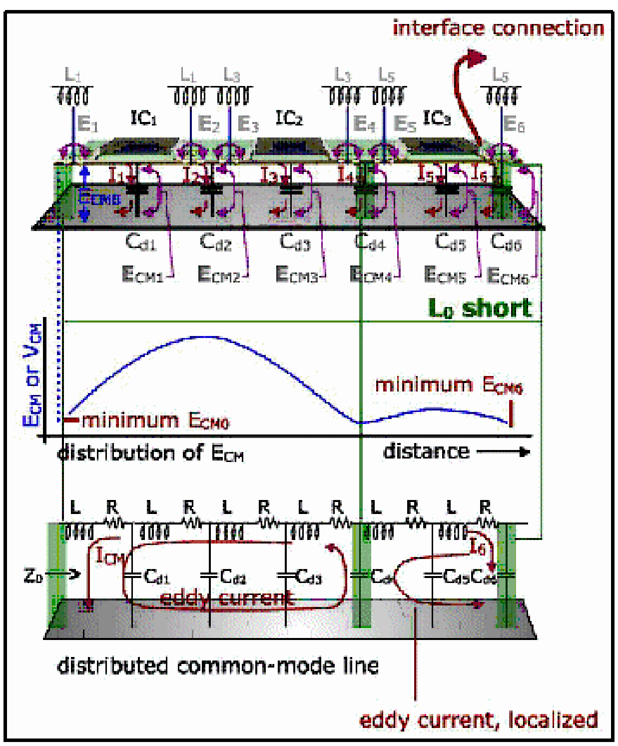

Figure Ten
Common-mode Potentials Redirected as "Intentional" Eddy Currents
Through Reflective "Null" Mismatches Within Impedance Flow Of Distributed Line
(Wave Transfer Impedance)

Another effect may be observed in the process represented by **Figure Ten**: The common-mode potentials developed across the circuit board are being *partially shunted* by the common-mode impedance of the chassis plane. From this observation it is possible to conclude that the common-mode performance of the circuit board itself would have been improved! A caution is appropriate to note in utilizing these techniques: the null formations establish intended common-mode eddy currents. Those common-mode currents will circulate in a pattern across the surface of the chassis plane *back up through the circuit board*. The conclusion yielded from this observation is that caution must be used in locating the nulls in order that the intended (redirected) common-mode currents will protect, not invade, sensitive circuit regions!

With appropriate implementation, it is indeed possible to improve common-mode performance utilizing the techniques represented. The performance improvement includes increasing signal-to-noise performance, particularly across sensitive partitions, and accordingly the EMC within the system-product itself.

This technical article is by W. Michael King **www.systemsEMC.com**